REMARKS

Claims 1-38 are currently pending in the Application. Claims 1, 18, and 27-30 are currently amended to clarify the claimed invention as embodied in these claims, without acquiescence or prejudice to pursue the original claims in a related application. No new matter has been added.

I. Claim Rejections Under 35 U.S.C. § 101

Claims 28, 30, 33-34, and 37-38 stand rejected under 35 U.S.C. § 101 as being allegedly directed to non-statutory subject matter.

Without acquiescence in the cited basis for rejection, claims 28 and 30 are currently amended. Applicants respectfully submit that the current amendment to claims 28 and 30 are believed to render the rejections under 35 U.S.C. § 101 moot. Applicants thus respectfully request withdrawal of the rejections and reconsideration of these claims.

II. Claim Rejections Under 35 U.S.C. § 102(b)

Claims 1-7, 12-13, 15-17, 27-28 and 31-34 stand rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 6,182,258 issued to Hollander et al. (hereinafter Hollander.) Applicants respectfully traverse the rejections.

A. According to the Office action, items 170 and 172 of Fig. 5 of Hollander disclose respectively the claimed limitations of "*the HDL portion*" and "*the general programming language portion*". Applicants respectfully disagree.

Applicants first respectfully submit that "[a] claim is anticipated only if **each and every element as set forth in the claim is found**, either expressly or inherently described . . . ." MPEP § 2131 (emphasis added.) MPEP further mandates that "[t]he **identical invention must be shown in as complete detail** as is contained in the . . . claim" and that "[t]he **elements must be arranged as required by the claim** . . . ." MPEP 2131 (emphasis added.)

Claim 1 recites "an electrical design having both an HDL portion" and "a general programming language portion". In contrast, although Hollander discloses that item 170 constitute a Verilog model of the DUT, col. 10, l. 35, 172 is, however, part of the co-verification extension module 174 which is built on top of the apparatus 166 including a UNIX socket 176 and two protocol software layers 178 and 180. Col. 10, ll. 51-52. That is, 170 discloses a Verilog model of the design under test (DUT); and 172 discloses the "cycle-accurate model of the hardware apparatus" (172). Therefore, 170 and 172 **cannot disclose** different portions (the HDL portions and the general programming language portion) of a same electrical design.

As to the external software program 163, Applicants respectfully submit that 163 is merely another piece of software which is "run at full speed until it reaches pre-designated points at which the program interacts with the DUT. A co-verification request is then sent through the socket to the invention." Col. 10, ll. 44-47. Nowhere does Hollander disclose that the external software program 163 constitutes a portion of the electronic design of which the Verilog model is a part. Moreover, Applicants respectfully submit that the fact that Hollander discloses that the external software program 163 is "compiled and executed by the hardware apparatus while the DUT simulation is run simultaneously", col. 10, ll. 40-42, clearly shows that the external software program and the Verilog model are not two portions of the same electronic design.

As such, Applicants respectfully submit that Hollander does not disclose at least the above limitations and thus may not be used to preclude the patentability of claims 1-7, 12-13, 15-17, 27-28 and 31-34 for at least the foregoing reasons.

B. Applicants respectfully submit that Hollander does not disclose "*handling, with the external debugger, a simulator request for the simulator that is interrupted, the external debugger calling a request processing function at the simulator, the simulator request for simulation of the HDL*" of claim 1.

According to the Office action, col. 5, ll. 44-48, col. 9, ll. 58-65, col. 10, ll. 35-36 and ll. 50-56 of Hollander disclose the above limitations. Applicants respectfully disagree.

Applicants respectfully submit that Hollander discloses a test generation apparatus (162 in Fig. 4 or 166 in Fig. 5) which interfaces with both the DUT (170) and the co-verification module (174). The test generation module 174 stays available for both the inputs to the DUT (for simulation) and the inputs to the external software program 163 (for co-verification). Col. 10, ll. 59-61 and Figs. 4-5. Nonetheless, to the extent that the final Office action considers Hollander's "apparatus 162 and 166 as disclosing the claimed limitation of "external debugger", which Applicants respectfully disagree, Applicants respectfully submit that Hollander appears to be absolutely silent on the apparatus 162 or 166 handling a simulator request which is for the simulation of the HDL portion. That is, Hollander merely discloses the generation of tests for the inputs of both the DUT and the co-verification module but never discloses that the co-verification module or any part therein handles the simulator request for the simulator.

Claim 1 is currently amended to clarify the claimed invention, without acquiescence in the cited basis for rejection or prejudice to pursue the original claim in a related application.

C. Applicants further respectfully submit that Hollander does not disclose the claimed limitations of "interrupting a simulator that operates upon the HDL portion of the electronic design to allow for debugging of the HDL portion, the simulator interrupted by an external debugger, the external debugger debugging the general programming language portion of the electronic design".

Applicants again respectfully point out that "[a] claim is anticipated only if **each and every element as set forth in the claim is found**, either expressly or inherently described . . . ." MPEP § 2131 (emphasis added.) MPEP further mandates that "[t]he **identical invention must be shown in as complete detail** as is contained in the . . . claim" and that "[t]he **elements must be arranged as required by the claim** . . . ." MPEP 2131 (emphasis added.)

The final Office action cites to col. 5, ll. 44-48, col. 9, 12-13, col. 10, ll. 35-36 and 50-56 and alleges that these cited passages disclose the claimed limitation of "interrupting a simulator that operates upon the HDL portion . . . by an external debugger to debug the general programming language portion of the electronic design" of claim 1. Applicants respectfully disagree for the following reasons.

(a) **Col. 5, ll. 44-48:**

These passages disclose that "[t]he **user can set breakpoints in the hardware-oriented verification-specific object-oriented programming language code**, and can observe and change variable values inside both the verification-specific object-oriented language and the

HDL code. The user can also use the invention to generate customized reports detailing the debugging process." (Emphasis added.) These passages merely disclose that it is the user who can set some breakpoints, not within the HDL code, but in the hardware-oriented verification-specific object-oriented programming language code. This aspect of setting breakpoints in an object-oriented programming language code is a commonly known manual debug process and has absolutely no bearing on "interrupting a simulator that operates upon the HDL portion of the electronic design . . . by an external debugger".

(b) **Col. 9, ll. 11-12:**

These passages show that the results of the generated tests by the apparatus 162 or 166 may be used in debugging the DUT with or without user input. Col. 9, ll. 1-15. However, these passages remain absolutely silent on and has no bearing on the claimed limitation of "interrupting the simulator . . . by an external debugger".

(c) **col. 10, ll. 35-36:**

Col. 10, ll. 35-40 discloses that the test generation apparatus 166 interfaces with the Verilog model 170 of the DUT and a Unix socket through some protocol software layer. Nonetheless, these passages remain absolutely silent on and has no bearing on the claimed limitation of "interrupting the simulator . . . by an external debugger".

(d) **Col. 10, ll. 50-56:**

These passages of Hollander disclose that the co-verification extension module 174 is built on top of the herein described apparatus, and that test generation, checking, debugging,

coverage, and reporting all combine information from both the hardware and the software sides. Nonetheless, these passages remain absolutely silent on and has no bearing on the claimed limitation of "interrupting the simulator . . . by an external debugger".

(e) Fig. 6, element 90 and col. 10, ll. 44-50:

The final Office action further cites to item 90 in Fig. 6 and col. 10, ll. 44-50 and alleges that since Hollander discloses "stop on errors" and "breakpoints", Hollander thus discloses the above claimed limitations. Applicants respectfully disagree.

The cited passages in col. 10 disclose that a co-verification request is sent to the test generation apparatus 166 via the Unix socket, that the test generation apparatus interprets the request and executes some functions, and that the results are returned to the external program 163 in the co-verification extension module 174. Nonetheless, all the above are limited between the co-verification extension module 174 and the test generation apparatus 166 yet has nothing to do with "interrupting the simulator that operates upon the HDL portion . . . by an external debugger to debug the general programming language portion . . ." of claim 1.

Moreover, Fig. 6 merely shows "stop on errors" under the Debug menu. Nonetheless, this "stop on error" does not disclose at least the limitation of "interrupting a simulator that operates upon the HDL . . . by an external debugger to debug the general programming language portion . . ." of claim 1.

As such, Applicants respectfully submit that Hollander does not disclose at least the aforementioned limitations and thus may not be used to prevent the patentability of claims 1,

III. Claim Rejections Under 35 U.S.C. § 103(a)

Claims 8-11 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Hollander in view of U.S. Patent No. 6,466,898 issued to Chan et al. (hereinafter Chan.) Applicants respectfully traverse the rejections.

Applicants respectfully submit that because the final Office action does not rely on Chan in forming the grounds for rejections of claims 1 from which claims 8-11 depend and because Hollander does not explicitly or inherently disclose all the claimed limitations of claim 1, Hollander and Chan, either alone or combined, do not disclose, teach, or suggest all the limitations of claims 8-11 and thus may not be used to preclude their patentability under 35 U.S.C. § 103(a) for at least this reason and the reasons presented in section II above.

IV. Claim Rejections Under 35 U.S.C. § 103(a)

Claim 14 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Hollander in view of Stallman et al, "Debugging with GDB: The GNU Source-Level Debugger", Jan. 2002 (hereinafter Stallman.) Applicants respectfully traverse the rejections.

Applicants respectfully submit that because the final Office action does not rely on Stallman in forming the grounds for rejections of claims 1 from which claim 14 depends and because Hollander does not explicitly or inherently disclose all the claimed limitations of claim 1, Hollander and Stallman, either alone or combined, do not disclose, teach, or suggest all the limitations of claim 14 and thus may not be used to preclude its patentability under 35 U.S.C. § 103(a) for at least this reason and the reasons presented in section II above.

V. Claim Rejections Under 35 U.S.C. § 103(a)

Claims 18-23, 25-26, 29-30, 36, and 38 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Hollander in view of Chan. Applicants respectfully traverse the rejections.

As similarly presented in subsection II above, Applicants respectfully submit that Hollander and Chan, either alone or combined, do not disclose at least the following claimed limitations of claim 18. Claims 29-30 also recite similar limitations.

> processing the second language portion of the design **to cause an interruption** of processing for the first language portion of the design, wherein the processing for the first language portion is **interrupted to process the second language portion**;
>
> handling the one or more waiting requests for processing of the first language portion by having processing of the second language portion call a request processing function at the first language portion that has been interrupted, at least one of the one or more waiting requests for processing of the first language portion causes the processing of the first language portion;
>
> (emphasis added.)

A. Applicants respectfully submit that Hollander and Chan, either alone or combined, do not disclose, teach, or suggest the limitations of "the first language portion of the design" and "the second language portion of the design" for similar reasons as presented in subsection II-A above. Applicants further respectfully submit that Hollander and Chan do not disclose, teach, or suggest these limitations because the final Office action dose not rely on Chan in forming the basis for rejection of these claimed elements.

B. Applicants further respectfully submit that Hollander and Chan, either alone or combined, do not disclose the limitations of "handling the one or more waiting requests for processing of the first language portion by having processing of the second language portion call

a request processing function at the first language portion that has been interrupted, at least one of the one or more waiting requests for processing of the first language portion causes the processing of the first language portion" for similar reasons as presented in subsections II-B and II-C above. Applicants further respectfully submit that Hollander and Chan do not disclose, teach, or suggest these limitations because the final Office action dose not rely on Chan in forming the basis for rejection of these claimed elements.

As such, Applicants respectfully submit that Hollander and Chan do not disclose, teach, or suggest at least the aforementioned claimed limitations of claims 18-23, 25-26, 29-30, 36, and 38 and thus may not be used to preclude their patentability under 35 U.S.C. § 103(a) for at least the foregoing reasons. Claims 18-23, 25-26, 29-30, 36, and 38 are thus believed to be also allowable over Hollander and Chan.

CONCLUSION

Based on the foregoing, all claims are believed allowable, and an allowance of the claims is respectfully requested. If the Examiner has any questions or comments, the Examiner is respectfully requested to contact the undersigned at the number listed below.

Applicant(s) hereby explicitly retracts and rescinds any and all of the arguments and disclaimers presented to distinguish the prior art of record during the prosecution of all parent and related application(s)/patent(s), and respectfully requests that the Examiner re-visit the prior art that such arguments and disclaimers were made to avoid.

The Commissioner is authorized to charge any fees due in connection with the filing of this document to Vista IP Law Group's Deposit Account No. 50-1105, referencing billing number **7037682001**. The Commissioner is authorized to credit any overpayment or to charge any underpayment to Vista IP Law Group's Deposit Account No. 50-1105, referencing billing number **7037682001**.

Respectfully submitted,

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